UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,707	01/24/2002	Teruhiko Kamigata	1614.1210	7916

21171 7590 08/18/2008

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
DONAGHUE, LARRY D	

ART UNIT	PAPER NUMBER
2154	

MAIL DATE	DELIVERY MODE
08/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/053,707	KAMIGATA ET AL.	
	Examiner	Art Unit	
	Larry D. Donaghue	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-14 are presented for examination.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admission of prior art, (AAPA) pages 1-11 and figures 1-9 in view of Official Notice.

4. AAPA taught the invention substantially as claimed including identifying a classification of a functional unit which can execute a basic instruction ; determining whether said basic instruction can be assigned to a logical instruction slot through checking a relationship between said classification of said functional unit and said logical instruction slot (page 10. lines 6-23) : and assigning, to an instruction slot, said basic instruction determined to be assignable to said logical instruction slot (page 8, lines 30).

5. AAPA does not expressly teach a pointer, official notice is taken that a pointer is a conventional means for designating placement of data in a sequentially addressable memory location.

6. As to claim 2, AAPA taught that identifying is divided into identifying an instruction category of a basic instruction, and identifying a classification of a functional unit which can execute said instruction category (page 7, lines 6-36).

7. As to claim 3, AAPA taught that further comprising prior to said assigning, checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots (Page 8, lines 31-37).

8. As to claim 4, AAPA taught that prior to said assigning, for checking a relationship between said basic instruction that can be assigned to said logical instruction slot and other basic instructions to be assigned to other logical instruction slots (Page 8, lines 31-37).

9. As to claim 5, AAPA taught that identifying said logical instruction slot having a lowest numeral determined to be assignable (see figure 3 note time 2 and 3, clearly showing the basic instruction are placed in the slot having the lowest numeral).

10. As to claim 6, 13 and 14, AAPA taught the additional features of assigning includes identifying said logical instruction slot having a lowest numeral determined to be assignable (see figure 3, note time 2 and 3, clearly showing the basic instruction are placed in the slot having the lowest numeral).

11. As to claim 7, AAPA taught that identifying, determining, checking and assigning are repeated for all instruction slots (page 9, lines 1-12).

12. As to claim 8, AAPA taught that identifying, determining, checking and assigning are repeated for all instruction slots (page 9, lines 1-12).

13. Claims 9-14 are rejected for the same rational as claims 1-8, above.

Applicant's arguments filed 06/27/2008 have been fully considered but they are not persuasive.

Applicant has amended the claims to included wherein the logical instruction slot is an imaginary instruction slot which corresponds to the functional unit, as is recited in claim 1 of the present application. The limitation has no further defining value in appraising the novelty of the invention as neither the logical or imaginary instruction slot are the physical instruction slot. Therefore any reference to a logical instruction slot is equivalent to referencing an imaginary instruction slot. If there is some other meaning attached to elements referenced, applicant should detail this in response to this action.

Applicant argues "However, the Applicants respectfully submit that the Examiner has cited a conventional process of compiling VLIW code to be used in a VLIW processor. This is in direct contrast to determining whether said basic instruction *can* be assigned to a logical instruction slot,..wherein the logical instruction slot is an imaginary instruction slot which corresponds to the functional unit, as is recited in claim 1 of the present application. "

See comments above.

Applicant argues "Further, the Applicants respectfully submit that the Examiner has taken improper Official Notice in the Office Action. The Examiner has simply alleged that a pointer is a conventional means for designating placement of data in a sequentially addressable memory location. However, the Applicants respectfully submit that the recited features of claim 1 are not reciting any such typical pointer as discussed by the Examiner, and further that the Official Notice fails to recognize the novel use of a logical instruction slot pointer recited in claim 1. "

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Larry D. Donaghue whose telephone number is 571-272-3962. The examiner can normally be reached on M-F 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Larry D Donaghue/
Primary Examiner, Art Unit 2154